region between the source and drain regions, via at least the side surface of the convex semiconductor layer, the side-wall gate portion being offset with respect to a part of a lower portion of the source region and a part of a lower portion of the drain region.

IN THE ABSTRACT:

Please replace the Abstract originally filed with the attached substitute Abstract.

REMARKS

By the present Amendment, Applicant has canceled claim 22 without prejudice or disclaimer of the subject matter thereof, and amended claim 1 to more appropriately define the invention. Claims 1-21 and 23-45 are pending, with claims 3-21 and 24-34 being withdrawn from further consideration by an election of species.

In the Office Action, the Examiner rejected claim 1 under 35 U.S.C. § 112, second paragraph, as being indefinite; and rejected claims 1, 2, 22, 23, and 35-45 under 35 U.S.C. § 103(a) as unpatentable over Miyawaki et al. (U.S. Patent 5,567,962, hereinafter "Miyawaki"). Applicant traverses these rejections for the following reasons.

Response to 35 U.S.C. § 112, second paragraph, Rejection

In this rejection, the Examiner contends that claim 1 fails to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. The Examiner alleges that the phrase "the source and the drain region changes on the side surface of the convex semiconductor layer," is unclear. Applicant has amended claim 1 to remove the phrase "the source and the drain region changes on the side surface of the convex semiconductor layer," without conceding that the Examiner's allegation is

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correct. Applicant in no manner disclaims this subject matter and reserves the right to reintroduce this subject matter.

Response to 35 U.S.C. § 103(a) Rejections

In this rejection, the Examiner contends that Miyawaki discloses a semiconductor device comprising a convex semiconductor layer 1013/1016/1021, a source region 1030, a drain region 1017, and a gate electrode 1023 having a side-wall age portion 1023 provided over a side surface of the convex semiconductor layer (Office Action, p. 3). The Examiner admits that Miyawaki does not expressly disclose that the gate electrode has a side-wall gate portion in an insulated state with respect to the convex semiconductor layer and that the gate electrode applies an electric field effect to a channel between the source and drain regions, via at least the side surface of the convex semiconductor layer (Office Action, p. 3). The Examiner, however, alleges that "it would have been obvious ... to apply[sic] the voltage to the gate electrode to create the electric field effect to a channel region, because such transistor function is well known in the art," (Office Action, p. 3). Additionally, the Examiner alleges that Miyawaki discloses that the side-wall gate protion is offset with respect to part of the source region and the drain region (Office Action, p. 4). Applicant respectfully asserts that a *prima facie* case of obviousness has not been established for the following reasons.

Argue.

In order to establish a *prima facie* case of obviousness, three basic criteria must be met. First, the prior art reference (or references when combined) must teach or suggest all the claim elements. Furthermore, "[a]ll words in a claim must be considered in judging the patentability of that claim against the prior art." *See* M.P.E.P. § 2143.01 (8^{th} Ed., Aug. 2001), quoting *In re Wilson*, 424 F.2d 1382, 1385, 165 U.S.P.Q. 494, 496 (C.C.P.A. 1970).

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Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify a reference or to combine reference teachings. Third, there must be a reasonable expectation of success. *See* M.P.E.P. § 2143 (8^{th} Ed. 2001), pp. 2100-122 to 127. In this case, a *prima facie* case of obviousness has not been established because Miyawaki fails to teach all the claim elements.

Claim 1 is directed to a semiconductor device comprising a combination of elements including, *inter alia*, "a gate electrode having a side-wall gate portion provided over a side surface of the convex semiconductor layer, in an insulated state with respect to the convex semiconductor layer, the gate electrode applying an electric field effect to a channel region between the source and drain regions, via at least the side surface of the convex semiconductor layer, the side-wall gate portion being offset with respect to a part of a lower portion of the source region and a part of a lower portion of the drain region."

In contrast, Miyawaki does not teach or suggest a side-wall gate portion of a gate electrode being offset with respect to a part of a lower portion of the source region and a part of a lower portion of the drain region. Miyawaki discloses a gate electrode 1023 formed over a channel region 1021. *See* Miyawaki, Fig. 25. But, Miyawaki also discloses that the channel region 1021, illustrated in Fig. 25, is not uniformly formed. Moreover, Fig. 25 of Miyawaki illustrates a structure of a lightly doped drain (LDD) or gate overlapped drain (GOLD). As stated above, the Examiner argues "Miyawaki discloses a semiconductor device wherein the side-wall gate portion is offset with respect to a part of the source region and the drain region, fig. 25," (Office Action, p. 4).

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However, since Miyawaki illustrates in Fig. 25 an LDD or GOLD , the source region includes not only n+ region 1017 but also n- region 1085, and the drain region includes not only n+ region 1030 but also n- region 1085. Thus, n- regions 1085 are positioned underneath gate electrode 1023. This means that side-wall gate portions 1086 of gate electrode 1023 of Miyawaki are not offset with respect to a part of the lower portion of the source region and a part of the lower portion of the drain region.

Thus, Miyawaki does not teach or suggest at least "a gate electrode having a side-wall gate portion ... the side-wall gate portion being offset with respect to a part of a lower portion of the source region and a part of a lower portion of the drain region," as recited in claim 1. Therefore, a *prima facie* case of obviousness has not been established for claim 1. For at least this reason, claim 1 is allowable.

Furthermore, the Examiner alleges that "it would have been obvious ... to apply[sic] the voltage to the gate electrode to create the electric field effect to a channel region, because such transistor function is well known in the art," (Office Action, p. 3). Applicant is unclear how to interpret the Examiner's allegation "such transistor function is well known in the art." It appears that the Examiner may be attempting to take "Official Notice" to allege that certain elements of Applicant's claimed invention are "well known" in the art. Since the record is unclear, Applicant requests that the Examiner clarify the arguments presented in the rejection by further explaining the rejection of claim 1.

To the extent that the Examiner is, in fact, relying on taking "Official Notice" in stating these conclusions, the Examiner is respectfully reminded of the provisions of M.P.E.P. § 2144.03, the procedures set forth in the Memorandum by Stephen G. Kunin,

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Deputy Commissioner for Patent Examination Policy dated February 21, 2002, and the precedents provided in *Dickinson v. Zurko*, 527 U.S. 150, 50 U.S.P.Q.2d 1930 (1999) and *In re Ahlert*, 424 F.2d, 1088, 1091, 165 U.S.P.Q. 418, 420 (CCPA 1970). An "Official Notice" rejection is improper unless the facts asserted are well-known or common knowledge in the art, and capable of instant and unquestionable demonstration as being well-known. Further, any facts asserted as well-known should serve only to "fill in the gaps" in an insubstantial manner. It is never appropriate to rely solely on "common knowledge" without evidentiary support in the record as the principal evidence upon which a rejection is based.

Applicants submit, in view of these provisions, that "a gate electrode ... in an insulated state with respect to the convex semiconductor layer, the gate electrode applying an electric field effect to a channel region between the source and drain regions, via at least the side surface of the convex semiconductor layer," *as set forth in the claims*, is not unquestionably well-known, and the Examiner has failed to demonstrate such. Further, considering the assertions on the record, it appears the Examiner is attempting to improperly rely on "Official Notice" as the basis upon which to justify the rejection. Accordingly, Applicants traverse the "Official Notice" and request that the Examiner withdraw the rejection and timely allow the pending claims. However, if the Examiner maintains his position that the pending claims are not allowable, Applicant requests that the Examiner cite a competent prior art reference in substantiation of these unsupported conclusions and set forth a proper rejection based on factual evidentiary support that is made of record.

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Furthermore, claim 2 is directed to a semiconductor device comprising a combination of elements including, *inter alia*, "a gate electrode having a side-wall gate portion provided over a side surface of [a] convex semiconductor layer, in an insulated state with respect to the convex semiconductor layer, the gate electrode applying an electric field effect to a channel region between the source and drain regions, via at least the side-wall gate portion." As advanced above, Applicant asserts that the Examiner has improperly rejected claim 2 because the Examiner has alleged that certain facts are well-known or common knowledge in the art, which are not capable of instant and unquestionable demonstration as being well-known. Thus, the Examiner is relying upon evidentiary support that is not of record. Hence, the rejection of claim 2 is improper. For at least this reason, claim 2 is allowable.

Moreover, claims 22, 23, and 35-45 are allowable at least due to their dependence from allowable claim 1. "If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious." M.P.E.P. § 2143.03, p. 2100-126 citing *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988).

In view of the foregoing, Applicant respectfully requests the reconsideration and reexamination of this application and the timely allowance of the pending claims.

Attached hereto is a marked-up version of the changes made to the title, specification, claims, and abstract by this Amendment. The attachment is captioned "**Appendix to Amendment of August 19, 2002**".

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Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: August 16, 2002

By: ______________________
Bryan S. Latham
Reg. No. 49,085

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IN THE TITLE:

Please change the title to read --[SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME] FIELD EFFECT TRANSISTOR USING SIDE-WALL GATES TO PREVENT PUNCH-THROUGH--.

IN THE SPECIFICATION:

Please amend the specification as follows:

Please delete the paragraphs beginning on page 5, line 16, and ending on page 18, line 25, and replace them with the following new paragraph:

[A semiconductor device according to a first aspect of the present invention comprises a convex semiconductor layer provided on a semiconductor substrate, a source region and a drain region provided in the convex semiconductor layer, a gate electrode has a side-wall gate portion provided over a side surface of the convex semiconductor layer, in an insulated state with respect to the convex semiconductor layer. The gate electrode applies an electric field effect to a channel region between the source and drain regions, via at least the side surface of the convex semiconductor layer. A distance between the source region and the drain region changes on the side surface of the convex semiconductor layer.

A semiconductor device according to a second aspect of the present invention comprises a convex semiconductor layer provided on a substrate, a source region and

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a drain region provided in the convex semiconductor layer, a gate electrode has a side-wall gate portion provided over a side surface of the convex semiconductor layer, in an insulated state with respect to the convex semiconductor layer, the gate electrode applies an electric field effect to a channel region between the source and drain regions, via at least the side surface of the convex semiconductor layer, and a side-wall insulating film provided on a side surface of the gate electrode and the side surface of the convex semiconductor layer.

A semiconductor device according to a third aspect of the present invention comprises a convex semiconductor layer provided on a substrate, a isolation film provided on a periphery of a lower portion region of the convex semiconductor layer, the position of the upper surface of the isolation film being lower than an upper surface of the convex semiconductor layer, a source region and a drain region provided in the convex semiconductor layer, the position of the deepest portion of the source region and the position of the deepest portion of the drain region is equal to or lower than the position of the upper surface of the isolation film, a gate electrode having a side-wall gate portion provided over a side surface of the convex semiconductor layer, in an insulated state with respect to the convex semiconductor layer, the gate electrode applies an electric field effect to a channel region between the source and drain regions, via at least the side surface of the convex semiconductor layer.

A semiconductor device according to a fourth aspect of the present invention comprises a first convex semiconductor layer provided on a substrate, the first convex semiconductor layer electrically connected to the substrate, a second convex semiconductor layer provided on the substrate, the second convex semiconductor layer

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electrically connected to the substrate, the second convex semiconductor layer having the same width as the first semiconductor layer, a first source region and a first drain region provided in the first convex semiconductor layer, a second source region and a second drain region provided in the second convex semiconductor layer, a gate electrode having a side-wall gate portion provided over a side surface of the first convex semiconductor layer and a side surface of the second convex semiconductor layer, in an insulated state with respect to the first and second convex semiconductor layers respectively, the gate electrode applies an electric field effect to a first channel region between the first source and drain regions and a second channel region between the second source and drain regions, via at least the side surfaces of the first and second convex semiconductor layer.

A semiconductor device according to a fifth aspect of the present invention comprises a first convex semiconductor layer provided on a substrate, the first convex semiconductor layer electrically connected to the substrate, a second convex semiconductor layer provided on the substrate, the second convex semiconductor layer electrically connected to the substrate, a first source region and a first drain region provided in the first convex semiconductor layer, a second source region and a second drain region provided in the second convex semiconductor layer, a first gate electrode having a first side-wall gate portion provided over a side surface of the first convex semiconductor layer, in an insulated state with respect to the first convex semiconductor layer, the first gate electrode applies an electric field effect to a first channel region between the first source and drain regions, via at least the side surface of the first convex semiconductor layer, a second gate electrode having a second side-wall gate

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portion provided over a side surface of the second convex semiconductor layer, in an insulated state with respect to the second convex semiconductor layer, the second gate electrode applies an electric field effect to a second channel region between the second source and drain regions, via at least the side surface of the second convex semiconductor layer, a first wiring electrically connected to the first source region and the second source region, a second wiring electrically connected to the first drain region and the second drain region and a third wiring electrically connected to the first gate electrode and the second gate electrode.

A semiconductor device according to a sixth aspect of the present invention comprises a first convex semiconductor layer provided on a substrate, a second convex semiconductor layer provided on the substrate;

a source region and a drain region provided in the first convex semiconductor layer, and a gate electrode having a side-wall gate portion provided over a side surface of the first convex semiconductor layer, in an insulated state with respect to the first convex semiconductor layer, and a gate contact portion provided over an upper surface of the second convex semiconductor layer, in an insulated state with respect to the second convex semiconductor layer, the gate electrode applies an electric field effect to a channel region between the source and drain regions, via at least the side surface of the first convex semiconductor layer.

A semiconductor device according to a seventh aspect of the present invention comprises a convex semiconductor layer provided on a substrate, a source region and a drain region provided in the convex semiconductor layer, and a gate electrode having a side-wall gate portion provided over a side surface of the convex semiconductor layer,

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in an insulated state with respect to the convex semiconductor layer, and a upper gate portion provided over an upper surface of the convex semiconductor layer, in an insulated state with respect to the convex semiconductor layer, the gate electrode applies an electric field effect to a channel region between the source and drain regions, via at least the side surface of the convex semiconductor layer. A conductive material of the side-wall gate portion is different from a conductive material of the upper gate portion.

A semiconductor device according to an eighth aspect of the present invention comprises a convex semiconductor layer provided on a substrate, a source region and a drain region provided in the convex semiconductor layer, a gate electrode having a side-wall gate portion provided over a side surface of the convex semiconductor layer, in an insulated state with respect to the convex semiconductor layer, and a upper gate portion provided over an upper surface of the convex semiconductor layer, in an insulated state with respect to the convex semiconductor layer, the gate electrode applies an electric field effect to a channel region between the source and drain regions, via at least the side surface of the convex semiconductor layer, and a wiring being electrically connected to the upper gate portion above the upper surface of the convex semiconductor layer.

A semiconductor device according to a ninth aspect of the present invention comprises a first convex semiconductor layer provided on a substrate, a second convex semiconductor layer provided on the substrate, a first source region and a first drain region provided in the first convex semiconductor layer, a second source region and a second drain region provided in the second convex semiconductor layer, a gate

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electrode having a side-wall gate portion provided over a side surface of the first convex semiconductor layer and a side surface of the second convex semiconductor layer, in an insulated state with respect to the first and second convex semiconductor layers respectively, the gate electrode applies an electric field effect to a first channel region between the first source and drain regions and a second channel region between the second source and drain regions, via at least the side surfaces of the first and second convex semiconductor layer, and at least one third convex semiconductor layer electrically connected to at least either the first and the second source regions, or the first and the second drain regions.

A semiconductor device according to a tenth aspect of the present invention comprises a first convex semiconductor layer provided on a substrate, a second semiconductor layer provided on the substrate, a first source region and a first drain region of a first conductive type provided in the first semiconductor layer, a second source region and a second drain region of a second conductive type provided in the second convex semiconductor layer, a depth of the second source region and a second drain region being deeper than the depth of the first source region and the second drain region, a first gate electrode having a first side-wall gate portion provided over a side surface of the first convex semiconductor layer, in an insulated state with respect to the first convex semiconductor layer, the first gate electrode applies an electric field effect to a first channel region between the first source and drain regions, via at least the side surface of the first convex semiconductor layer, a second gate electrode having a second side-wall gate portion provided over a side surface of the second convex semiconductor layer, in an insulated state with respect to the second convex

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semiconductor layer, the second gate electrode applies an electric field effect to a second channel region between the second source and drain regions, via at least the side surface of the second convex semiconductor layer.

A semiconductor device according to an eleventh aspect of the present invention comprises a first convex semiconductor layer provided on a substrate, a second convex semiconductor layer provided on the substrate, a first source region and a first drain region provided in the first convex semiconductor layer, a second source region and a second drain region having the same conductive type as the first source region and the first drain region provided in the second convex semiconductor layer, a depth of the first source region and a depth of the second drain region being deeper than the first source region and the second drain region, a first gate electrode having a first side-wall gate portion provided over a side surface of the first convex semiconductor layer, in an insulated state with respect to the first convex semiconductor layer, the first gate electrode applies an electric field effect to a first channel region between the first source and drain regions, via at least the side surface of the first convex semiconductor layer, and a second gate electrode having a second side-wall gate portion provided over a side surface of the second convex semiconductor layer, in an insulated state with respect to the second convex semiconductor layer, the second gate electrode applies an electric field effect to a second channel region between the second source and drain regions, via at least the side surface of the second convex semiconductor layer.

A semiconductor device according to a twelfth aspect of the present invention comprises a convex semiconductor layer provided on a substrate, a source region and a drain region provided in the convex semiconductor layer, and a gate electrode having

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a side-wall gate portion provided over a side surface of the convex semiconductor layer, in an insulated state with respect to the convex semiconductor layer, the gate electrode applies an electric field effect to a channel region between the source and drain regions, via at least the side surface of the convex semiconductor layer, the gate electrode including at least a first layer and a second layer. The gate electrode uses a word line of a semiconductor memory device.

A semiconductor device according to a thirteenth aspect of the present invention comprises a convex semiconductor layer provided on a substrate, a source region and a drain region provided in the convex semiconductor layer, and a gate electrode having a side-wall gate portion provided over a side surface of the convex semiconductor layer, in an insulated state with respect to the convex semiconductor layer, the gate electrode applies an electric field effect to a channel region between the source and drain regions, via at least the side surface of the convex semiconductor layer, the gate electrode including at least a first layer and a second layer. An upper surface of the first layer is planar and the second layer is provided on the upper surface of the first layer.

A semiconductor device according to a fourteenth aspect of the present invention comprises a convex semiconductor layer provided on a substrate, a source region and a drain region provided in the convex semiconductor layer, and a gate electrode having a side-wall gate portion provided over a side surface of the convex semiconductor layer, in an insulated state with respect to the convex semiconductor layer, the gate electrode applies an electric field effect to a channel region between the source and drain regions, via at least the side surface of the convex semiconductor layer, the gate electrode including at least a first layer and a second layer. An upper surface of the first layer has

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a step, the second layer is provided on the upper surface of the first layer, and an upper surface of the second layer is planar.

A semiconductor device according to a fifteenth aspect of the present invention comprises a convex semiconductor layer provided on a substrate, the convex semiconductor having a first side surface, a second side surface opposite to the first side surface, a third side surface located between the first and second side surface, a forth side surface opposite to the third surface, and a upper surface, a source region and a drain region provided in the convex semiconductor layer, the source region and the drain region including an electric contact portion respectively, the electric contact portion extending over a part of the first side surface, a part of the upper surface, a part of the second side surface and either of parts of the third and fourth side surfaces, a gate electrode having a side-wall gate portion provided over a side surface of the convex semiconductor layer, in an insulated state with respect to the convex semiconductor layer, the gate electrode applies an electric field effect to a channel region between the source and drain regions, via at least the side surface of the convex semiconductor layer.

A semiconductor device according to a sixteenth aspect of the present invention comprises a convex semiconductor layer provided on a substrate, a source region and a drain region provided in the convex semiconductor layer, and a gate electrode having a side-wall gate portion provided over a side surface of the convex semiconductor layer, in an insulated state with respect to the convex semiconductor layer, and a upper gate portion provided over an upper surface of the convex semiconductor layer, in an insulated state with respect to the convex semiconductor layer, the gate electrode

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applies an electric field effect to a channel region between the source and drain regions, via at least the side surface of the convex semiconductor layer. A gate length of the side-wall gate portion is shorter than the gate length of the upper gate portion.

A method of manufacturing a semiconductor device according to a first aspect of the present invention comprising: etching a semiconductor substrate to form a convex semiconductor layer on the semiconductor substrate; forming a gate insulating film at least on a side surface of the convex semiconductor layer; forming a gate electrode on the gate insulating film; forming a side-wall insulating film on a side surface of the gate electrode and on the side surface of the convex semiconductor layer; and introducing impurity into the convex semiconductor layer by using at least the gate electrode and the side-wall insulating film as a mask to form a source region and a drain region in the convex semiconductor layer.

A method of manufacturing a semiconductor device according to a second aspect of the present invention comprising: forming an insulating film having an open hole on a semiconductor substrate; forming a convex semiconductor layer on a semiconductor substrate exposed from the open hole; forming a gate insulating film on at least a side surface of the convex semiconductor layer; forming a gate electrode on the gate insulating film; and introducing impurity into the convex semiconductor layer by using at least the gate electrode as a mask to form a source region and a drain region in the convex semiconductor layer.

A method of manufacturing a semiconductor device according to a third aspect of the present invention comprising: forming a convex semiconductor layer on a substrate; forming an insulator at a periphery of the convex semiconductor layer;

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forming a trench to form a side-wall gate portion in the insulator; forming a gate insulating film on a side surface of the convex semiconductor layer exposed at least from the trench; forming a gate electrode having a side-wall gate portion formed in the trench; and introducing impurity into the convex semiconductor layer by using at least the gate electrode as a mask to form a source region and a drain region in the convex semiconductor layer.]

--A semiconductor device according to an aspect of the present invention comprises: a convex semiconductor layer provided on a semiconductor substrate; a source region and a drain region provided in the convex semiconductor layer; and

a gate electrode having a side-wall gate portion provided over a side surface of the convex semiconductor layer, in an insulated state with respect to the convex semiconductor layer, the gate electrode applying an electric field effect to a channel region between the source and drain regions, via at least the side surface of the convex semiconductor layer, the side-wall gate portion being offset with respect to a part of the lower portion of the source region and a part of the lower portion of the drain region.--

Please replace the paragraph beginning on page 22, line 9, with the following new paragraph:

FIG. 24 is a sectional view showing a variation of a gate insulating film of the MOSFET according to the embodiments of the present invention.

Please replace the paragraph beginning on page 22, line 24, with the following new paragraph:

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FIG. 29 is a sectional view showing a variation of a source/drain region of the MOSFET according to <u>the embodiments of</u> the present invention.

Please replace the paragraph beginning on page 27, line 15, with the following new paragraph:

FIG. 62 is a perspective view showing a contact portion of the MOSFET according to <u>the embodiments of</u> the present invention.

Please replace the paragraph beginning on page 27, line 18, with the following new paragraph:

FIG. 63A is a plan view showing the contact portion of the MOSFET according to <u>the embodiments of</u> the present invention; FIG. 63B is a side view as seen form a direction of an arrow B shown in FIG. 63A; and FIG. 63C is a side view as seen from the direction of an arrow C shown in FIG. 63A.

<u>IN THE CLAIMS:</u>

Please amend claim 1 as follows:

1. (Amended) A semiconductor device comprising:

a convex semiconductor layer provided on a semiconductor substrate;

a source region and a drain region provided in the convex semiconductor layer; and

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a gate electrode having a side-wall gate portion provided over a side surface of the convex semiconductor layer, in an insulated state with respect to the convex semiconductor layer, the gate electrode applying an electric field effect to a channel region between the source and drain regions, via at least the side surface of the convex semiconductor layer, the side-wall gate portion being offset with respect to a part of a lower portion of the source region and a part of a lower portion of the drain region.

[wherein a distance between the source region and the drain region changes on the side surface of the convex semiconductor layer.]

IN THE ABSTRACT:

Please replace the Abstract originally filed with the attached new Abstract.

A semiconductor device [comprises] includes a convex semiconductor layer provided on a semiconductor substrate, a source region and a drain region provided in the convex semiconductor layer, and a gate electrode[. The gate electrode has] having a side-wall gate portion provided over a side surface of the convex semiconductor layer. The side-wall gate portion of the gate electrode is offset with respect to a part of the lower portion of the source region and a part of the lower portion of the drain region [in an insulated state with respect to the convex semiconductor layer].

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